

CLAIMS

1 1. (currently amended) A digital filter, comprising:
2 at least two multiple stage shift registers;
3 a plurality of multipliers corresponding in number to the number of stages in the at least two
4 multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at
5 least two multiple stage shift registers:
6 a tap weight shifter coupled to a tap weight source to receive tap weights, the tap weight shifter
7 coupled to provide a second input to each multiplier, the tap weight shifter capable of shifting tap
8 weights, each multiplier producing an output corresponding to a product of the first and second inputs;
9 and
10 an adder for summing the multiplier outputs to provide a sum output, wherein:
11 two or more sum outputs are generated between consecutive shiftings of new data into
12 the at least two multiple stage shift registers.

1 2. (original) A digital filter as recited in claim 1, further comprising:
2 a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage
3 buffer being coupled to provide inputs to the at least two multiple stage shift registers.

1 3. (original) A digital filter as recited in claim 2, wherein the multiple stage buffer is a
2 serial-input, parallel-output buffer.

1 4. (previously presented) A digital filter as recited in claim 1, wherein the tap weights
2 received by the tap weight shifter are one bit wide.

1 5. (previously presented) A digital filter as recited in claim 1, wherein the tap weights
2 received by the tap weight shifter are more than one bit wide and the tap weights have a bit width that is
3 no greater than a bit width of stages of the shift registers.

1 6. (original) A digital filter as recited in claim 1, wherein the digital filter is implemented
2 in software.

1 7. (original) A digital filter as recited in claim 1, wherein the digital filter is implemented
2 in an integrated circuit.

1 8. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented
2 in an application specific integrated circuit.

1 9. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented
2 in a digital signal processor.

1 10. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented
2 in a microcontroller.

1 11. (previously presented) A digital filter as recited in claim 7, wherein the digital filter is
2 implemented in a microprocessor.

1 12. (previously presented) A digital filter as recited in claim 1, further comprising the tap
2 weight source from which to receive the tap weights.

1 13. (original) A digital filter as recited in claim 12, wherein the tap weight source is random
2 access memory.

1 14. (original) A digital filter as recited in claim 12, wherein the tap weight source is
2 read-only memory.

1 15. (original) A digital filter as recited in claim 12, wherein the tap weight source is a
2 processor.

1 16. (currently amended) A receiver including a digital filter comprising:
2 at least two multiple stage shift registers;
3 a plurality of multipliers corresponding in number to the number of stages in the at least two
4 multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at
5 least two multiple stage shift registers:
6 a tap weight shifter coupled to a tap weight source to receive tap weights, the tap weight shifter
7 coupled to provide a second input to each multiplier, the tap weight shifter capable of shifting tap
8 weights, each multiplier producing an output corresponding to a product of the first and second inputs;
9 and
10 an adder for summing the multiplier outputs to provide a sum output, wherein:
11 two or more sum outputs are generated between consecutive shiftings of new data into
12 the at least two multiple stage shift registers.

1 17. (original) A receiver as recited in claim 16, further comprising:
2 a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage
3 buffer being coupled to provide inputs to the at least two multiple stage shift registers.

1 18. (original) A receiver as recited in claim 17, wherein the multiple stage buffer is a
2 serial-input, parallel-output buffer.

1 19. (previously presented) A receiver as recited in claim 16, wherein the tap weights
2 received by the tap weight shifter are one bit wide.

1 20. (previously presented) A receiver as recited in claim 16, wherein the tap weights
2 received by the tap weight shifter are more than one bit wide and the tap weights have a bit width that is
3 no greater than a bit width of stages of the shift registers.

1 21-26. (canceled)

1 27. (previously presented) A receiver as recited in claim 16, further comprising the tap
2 weight source from which to receive the tap weights.

1 28-30. (canceled)

1 31. (original) A receiver as recited in claim 16, wherein the receiver is a handset.

1 32. (original) A receiver as recited in claim 16, wherein the receiver is a base station.

1 33. (previously presented) A method of filtering digital data, comprising the steps of:
2 a. shifting digital data into first and second multiple stage shift registers;

- 3 b. multiplying an output from each stage of the first and second multiple stage shift
4 registers by an associated, respective tap weight to produce a plurality of products;
5 c. combining the plurality of products to form a sum;
6 d. circularly shifting the tap weights; and
7 e. repeating steps b and c at least once before step a is repeated.

1 34. (previously presented) A method of filtering digital data as recited in claim 33, further
2 comprising the step of shifting digital data into registers of a buffer prior to shifting the digital data into
3 first and second multiple stage shift registers.

- 1 35. (previously presented) A method of filtering data, comprising the steps of:
2 a. shifting data into N multiple stage shift registers, each of the N multiple stage shift
3 registers having at least L stages, N and L being integers, N being at least 2;
4 b. multiplying an output from each of the at least L stages of the N multiple stage shift
5 registers by a corresponding tap weight to produce a plurality of products;
6 c. combining the plurality of products to form a sum;
7 d. circularly shifting the tap weights;
8 e. repeating steps b, c, and d N-2 times before step a is repeated;
9 f. repeating steps b and c again before step a is repeated.

1 36. (previously presented) A method of filtering data as recited in claim 35, further
2 comprising the steps of
3 following step f, repeating steps a through f.

1 37. (original) A method of filtering data as recited in claim 35, further comprising the step
2 of shifting N pieces of data into registers of a buffer for temporary storage prior to shifting the N pieces
3 of data into respective ones of the N multiple stage shift registers.

1 38. (currently amended) A digital filter comprising:
2 N multiple-stage shift registers, $N > 1$;
3 a tap changer adapted to store a configuration of tap weights;
4 a plurality of multiplying elements, each multiplying element adapted to (a) receive (i) a datum
5 from a corresponding stage of a corresponding shift register and (ii) a corresponding tap weight from the
6 tap changer and (b) generate an output corresponding to a product of the datum and the corresponding tap
7 weight; and
8 an adder adapted to receive the output from each multiplying element and generate a sum
9 corresponding to the sum of the products of all of the data in the N multiple-stage shift registers and the
10 corresponding tap weights in the tap changer, wherein:
11 the digital filter is adapted to generate two or more different sums for each set of data
12 stored in the N multiple-stage shift registers; and
13 each different sum is based on a different configuration of tap weights in the tap changer.

1 39. (previously presented) The digital filter of claim 38, wherein:
2 the tap changer is a circular buffer; and
3 each different configuration of the tap weights is generated by circularly shifting the tap weights
4 within the tap changer.

1 40. (previously presented) The digital filter of claim 39, further comprising a tap weight
2 source adapted to reload an initial configuration of tap weights into the tap changer.

1 41. (previously presented) The digital filter of claim 40, wherein the tap weight source is
2 adapted to reload the initial configuration of tap weights after N sums have been generated based on N
3 different configurations of the tap weights.

1 42. (currently amended) The digital filter of claim 38, further comprising an input buffer
2 adapted to parallelize an incoming serial data stream for input into the N multiple-stage shift registers,
3 wherein each shift register is adapted to receive a corresponding portion of the incoming serial data
4 stream.

1 43. (currently amended) The digital filter of claim 42, wherein the digital filter is adapted to
2 generate N different sums based on N different configurations of the tap weights for each shift of
3 parallelized data into the N multiple-stage shift registers.

1 44. (currently amended) The digital filter of claim 38, wherein the N multiple-stage shift
2 registers do not all have the same number of stages.

1 45. (currently amended) The digital filter of claim 38, wherein the bit-width of each tap
2 weight is smaller than the bit-width of each datum in the N multiple-stage shift registers.

1 46. (currently amended) A receiver including a digital filter, the digital filter comprising:
2 N multiple-stage shift registers, $N > 1$;
3 a tap changer adapted to store a configuration of tap weights;
4 a plurality of multiplying elements, each multiplying element adapted to (a) receive (i) a datum
5 from a corresponding stage of a corresponding shift register and (ii) a corresponding tap weight from the
6 tap changer and (b) generate an output corresponding to a product of the datum and the corresponding tap
7 weight; and
8 an adder adapted to receive an output from each multiplying element and generate a sum
9 corresponding to the sum of the products of all of the data in the N multiple-stage shift registers and the
10 corresponding tap weights in the tap changer, wherein:
11 the digital filter is adapted to generate two or more different sums for each set of data
12 stored in the N multiple-stage shift registers; and
13 each different sum is based on a different configuration of tap weights in the tap changer.